

B O X A P

IN THE UNITED STATES PATENT AND TRADE MARKS OFFICE

Applicant: R.C. Foss et al  
 Serial No: 07/680,747  
 Filed: April 5, 1991  
 Title: METHOD FOR DRAM SENSING CURRENT CONTROL  
 Art Unit: 2502  
 Examiner: T. Dinh  
 Our File: 628.30050X00

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**NOT ENTERED**

The Commissioner of Patents  
 and Trade Marks,  
 Washington, D.C., 20231  
 U.S.A.

October 18, 1993

Dear Sir:

This is in response to the official action dated  
 May 17th, 1993 in the above-identified application.

Please amend the claims as follows:

1. (Amended) A dynamic random access memory  
 (DRAM) comprising:

- (a) a plurality of bit storage capacitors,
- (b) a folded bit line comprised of a complementary  
 bit line pair for receiving charge stored on one of said  
 capacitors, having bit line capacitance,
- (c) a sense amplifier having a pair of sense nodes  
 for sensing a voltage differential across said sense nodes,
- (d) high resistance controllable current leakage  
imperfect isolating means connecting said bit line to said

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